IN THE CLAIMS

Please amend the claims as follows:

Claims 1-16. (Canceled)

17. (Currently Amended) A method using a computer comprising:

adding legs to a transistor in a source layout to create a re-legged layout that violates design rules; and

performing compaction to modify the re-legged layout to comply with the design rules[[.]];

wherein adding legs to a transistor comprises forming a plurality of slots in a gate of the transistor.

18. (Canceled)

19. (Currently Amended) The method of claim ~~18~~ 17 further comprising expanding the gate of the transistor prior to forming the plurality of slots.

20. (Currently Amended) The method of claim ~~18~~ 17 further comprising placing contact seeds in areas uncovered by the plurality of slots.

21. (Currently Amended) ~~The method of claim 17 further comprising~~ A method using a computer comprising:

adding legs to a transistor in a source layout to create a re-legged layout that violates design rules;

performing compaction to modify the re-legged layout to comply with the design rules; and

determining a number of legs to add to the transistor according to:

$$N_{new} = \max\{N_{old}, \lceil (W_{old} \times f)/W_m \rceil\}$$

N_{new} - New number of legs.

W_{old} - Device width before resizing.

N_{old} - Old number of legs.

f - Upsize factor

W_m - Maximal leg size in new layout.

22. (Previously Presented) The method of claim 21 wherein determining a number of legs further comprises correcting the number of legs to add an even number of legs according to:

$$N_{new(corrected)} = N_{old} + \lfloor (N_{new} - N_{old} + 1)/2 \rfloor \times 2$$

23. (Currently Amended) ~~The method of claim 17~~ A method using a computer comprising:

adding legs to a transistor in a source layout to create a re-legged layout that violates design rules, wherein adding legs to a transistor in a source layout comprises adding legs to a transistor in a hard intellectual property (IP) layout source design[[.]]; and

performing compaction to modify the re-legged layout to comply with the design rules.

24. (Currently Amended) ~~The method of claim 17 further comprising~~ A method using a computer comprising:

adding legs to a transistor in a source layout to create a re-legged layout that violates design rules;

performing compaction to modify the re-legged layout to comply with the design rules; and

adding jogs to the source layout.

25. (Previously Presented) A method using a computer to add legs to a transistor in a source layout comprising:

inserting a plurality of slots into the layout upon a gate area of the transistor;

mathematically subtracting area of the plurality of slots from a poly layer without regard to satisfying design rules; and

placing contact seeds in diffusion areas uncovered by the subtracting, wherein the contact seeds are placed without regard to satisfying the design rules.

26. (Previously Presented) The method of claim 25 further comprising running an automated design tool on the source layout to modify dimensions of the transistor to satisfy the design rules.

27. (Previously Presented) The method of claim 26 wherein running an automated design tool on the source layout comprises running a compaction tool.

28. (Previously Presented) The method of claim 25 further comprising enlarging the gate area of the transistor prior to inserting a plurality of slots into the source layout.

29. (Previously Presented) The method of claim 25 further comprising determining a number of legs to add to the transistor according to:

$$N_{new} = \max\{N_{old}, \lceil (W_{old} \times f)/W_m \rceil\}$$

N_{new} - New number of legs.

W_{old} - Device width before resizing.

N_{old} - Old number of legs.

f - Upsize factor

W_m - Maximal leg size in new layout.

30. (Previously Presented) The method of claim 29 wherein determining a number of legs further comprises correcting the number of legs to add an even number of legs according to:

$$N_{new(corrected)} = N_{old} + \lfloor (N_{new} - N_{old} + 1)/2 \rfloor \times 2$$

31. (Previously Presented) The method of claim 25 wherein adding legs to a transistor in a source layout comprises adding legs to a transistor in a hard intellectual property (IP) layout source design.

32. (Previously Presented) The method of claim 25 further comprising adding jogs to the source layout.

33. (Previously Presented) A machine-readable medium containing instructions, which when executed, cause the following to be performed:

inserting a plurality of slots into a source layout upon a gate area of a transistor;

mathematically subtracting area of the plurality of slots from a poly layer without regard to satisfying design rules; and

placing contact seeds in diffusion areas uncovered by the subtracting, wherein the contact seeds are placed without regard to satisfying the design rules.

34. (Previously Presented) The machine-readable medium of claim 33 wherein the instructions, when executed, further cause a compaction tool to run on the source layout to modify dimensions of the transistor to satisfy the design rules.

35. (Previously Presented) The machine-readable medium of claim 34 wherein the instructions, when executed further cause determining a number of legs to add to the transistor according to:

$$N_{new} = \max\{N_{old}, \lceil (W_{old} \times f)/W_m \rceil\}$$

N_{new} - New number of legs.

W_{old} - Device width before resizing.

N_{old} - Old number of legs.

f - Upsize factor

W_m - Maximal leg size in new layout.

36. (Previously Presented) The machine-readable medium of claim 35 wherein determining a number of legs further comprises correcting the number of legs to add an even number of legs according to:

$$N_{new(corrected)} = N_{old} + \lfloor (N_{new} - N_{old} + 1)/2 \rfloor \times 2$$